Investigation of Variable Frequency ISPWM Control Method for an Asymmetric Multilevel Inverter

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Abstract— Multilevel inverter is an effective and practical solution for increasing power and reducing harmonics of ac waveforms. Several multilevel topologies are reported and the most popular topology is Cascaded Multilevel Inverter (CMLI). This paper focuses on asymmetric cascaded multilevel inverter employing variable frequency inverted sine PWM technique (VFISPWM). This technique combines the advantage of inverted rectified sine wave and variable frequency carriers for a seven level inverter for balancing the switch utilization. A detailed study of the technique was carried out through MATLAB/SIMULINK for switching losses and THD. Furthermore, a PI controller is used to control the MLI using the proposed PWM technique. The results were verified experimentally and FPGA processor is used for PWM. It was noticed that the proposed modulation strategy results in lower switching losses for a chosen THD as compared to the conventional strategies.

Index Term— Asymmetric Multilevel Inverter, Variable frequency ISPWM, Switching Loss.

I. INTRODUCTION
Multilevel inverters are mainly utilized to synthesize a desired voltage wave shape from several levels of dc voltages. Their main advantages are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency capability to operate at high voltages and modularity. Three topologies have been reported for multilevel inverters: Diode- clamped, flying capacitor and cascaded H-bridge [1]. The topology considered for this work is the cascaded H-bridge inverter which requires several independent dc sources. Normally, each phase of a cascaded multilevel inverter requires “n” dc sources for 2n+1 level. For many applications, multiple dc sources are required demanding long cables and this could lead to voltage unbalance among the dc sources. With an aim to reduce the number of dc sources required for the cascaded multilevel inverter for a motor drive, this paper focuses on asymmetric cascade MLI that uses two unequal dc sources in each phase to generate a seven level equal step multilevel output [2]. This structure is favourable for high power applications since it provides higher voltage at higher modulation frequencies (where they are needed) with a low switching (carrier) frequency. It means low switching loss for the same total harmonic distortion (THD). It also improves the reliability by reducing the number of dc sources.

For the cascaded multilevel inverter there are several well known sinusoidal pulse width modulation strategies [3]. Compared to the conventional triangular carrier based PWM, the inverted rectified sine carrier PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping [4]. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been suggested [5]. This paper however, presents a novel variable frequency inverted rectified sine modulation technique (VFISPWM) for a seven – level inverter. This novel method combines the advantage of inverted sine and multi frequency carrier signals. The VFISPWM provides an enhanced fundamental voltage, lower total harmonic distortion (THD) and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique maximizes the output voltage and gives a low THD of 5.92%. A PID controller is employed to enhance the performance of the asymmetric MLI using the proposed modulation strategy. A comparative evaluation between the VFISPWM and the conventional modulation is also presented in terms of output voltage quality, power circuitry complexity, and total harmonic distortion (THD), weighted total harmonic distortion (WTHD) and implementation cost.

Both the MLI circuit topology and its new control scheme are described in detail and their performance is verified based on simulation and experimental results.

II. ASYMMETRIC CASCADED MULTILEVEL INVERTER
The seven - level cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H₁ consists of a separate DC source Vdc₁, whereas the second H-Bridge H₂ consists of a dc source Vdc₂/2 as shown in Fig.1. Let the output of H-Bridge-1 be denoted as v₁(t) and the output of H-Bridge-2 be denoted as v₂(t). Hence the total output voltage is given by
$v(t) = v_1(t) + v_2(t)$. By alternately opening and closing the switches $S_1$, $S_4$, and $S_2$, $S_3$ of H-Bridge-1 appropriately, output of H$_1$, $v_1(t)$, can be made equal to $+V_{dc}$, $0$, or $-V_{dc}$. Similarly, the output voltage of H-Bridge-2, $v_2(t)$, can be made equal to $-V_{dc}/2$, $0$, or $+V_{dc}/2$ by opening and closing the switches of H$_2$ [14]. Hence $v(t)$ takes values $-3/2V_{dc}$, $-V_{dc}$, $-1/2V_{dc}$, $0$, $+1/2V_{dc}$, $+V_{dc}$, $+3/2V_{dc}$ as shown in the Fig.2.

The advantages of the topology are:

- Reduced number of dc sources.
- High speed capability
- Low switching loss
- High conversion efficiency.

III. PROPOSED VARIABLE FREQUENCY INVERTED SINE PWM TECHNIQUE (VFISPWM)

The proposed control strategy replaces the conventional fixed frequency carrier waveform [6] by variable frequency inverted sine wave. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. But the main drawback is the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable frequency inverted sine carrier signals. In order to balance the number of active switching among the levels it is to vary the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all levels. The reference carrier frequency was chosen as $3950\text{Hz}$ as switching losses and THD both are low as shown in Fig.3.

With the carrier reference frequency of $3950\text{Hz}$ applied to the band-1, the new frequencies for bands 2 and 3 are assigned proportional to their respective slopes.

In Fig.4, the modulating wave is defined as

$$V(t) = \sin \theta$$  \hspace{1cm} (1)$$

The calculation of the slope values for the three bands is shown below:

$$\theta_1 = \sin^1 0 = 0 \text{ radians}$$  \hspace{1cm} (2)$$

$$\theta_2 = \sin^1 (1/3) = 0.339 \text{ radians}$$  \hspace{1cm} (3)$$

$$\theta_3 = \sin^1 (2/3) = 0.728 \text{ radians}$$  \hspace{1cm} (4)$$

$$\theta_4 = \sin^1 (1) = 1.5707 \text{ radians}$$  \hspace{1cm} (5)$$

Slope of C$_1$ = 1.00  \hspace{1cm} (6)$$

Slope of C$_2$ = 0.8716  \hspace{1cm} (7)$$
Slope of $C_3 = 0.404$ (8)

Frequency of $C_1 = 3950$Hz (9)

Frequency of $C_2 = 3443$Hz (10)

Frequency of $C_3 = 1596$Hz (11)

Using the slope values of the carrier band, the new frequencies are calculated and the carrier waveforms are shown in the Fig.5. Also, the new frequency values are verified with the dwell time calculation of the reference waveform [5]. The number of switching actions (8) is balanced for all the switches in the proposed PWM technique as shown in Table I:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Proposed VFISPWM</th>
<th>Conventional PWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_sw$</td>
<td>48</td>
<td>72</td>
</tr>
<tr>
<td>THD</td>
<td>5.92%</td>
<td>7.98%</td>
</tr>
</tbody>
</table>

The parameters chosen for simulation using the proposed PWM technique is shown below:

<table>
<thead>
<tr>
<th>S. No</th>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Main DC source voltage (Vdc)</td>
<td>200V</td>
</tr>
<tr>
<td>2</td>
<td>Modulation Index (ma)</td>
<td>1.00</td>
</tr>
<tr>
<td>3</td>
<td>New Carrier Frequency</td>
<td>3950Hz, 3443Hz &amp; 1596Hz.</td>
</tr>
<tr>
<td>4</td>
<td>Frequency modulation Ratio (m)</td>
<td>$m_3 = 79, m_2 = 69, m_1 = 32$.</td>
</tr>
<tr>
<td>5</td>
<td>Filter (Resonant Arm Type)</td>
<td>LC (L = 2.2mH C = 220uF)</td>
</tr>
<tr>
<td>6</td>
<td>Rated Output Frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>7</td>
<td>Reference Voltage</td>
<td>200V</td>
</tr>
</tbody>
</table>

a. PI Control

A PI Controller (proportional-integral controller) is a feedback controller which drives the plant to be controlled with a weighted sum of the error (difference between the output and desired set-point) and the integral of that value. The function of PI is to regulate the multilevel inverter so that it stays close to the nominal operating point in the presence of disturbances and noise. PI controller settings $k_p$ and $k_i$ are designed in this work using Ziegler- Nichols tuning technique. The designed values of $k_p$ and $k_i$ are 0.0135 and 18.5 respectively.

IV. SIMULATION RESULTS

The cascaded seven-level inverter is simulated using MATLAB/SIMULINK and switching signals are generated using S-function block by employing the proposed modulation strategy. The simulation is carried out for different modulation index and carrier frequency values [8]. The performance parameters considered for comparing the proposed PWM with the conventional method is the output voltage quality, THD, WTHD and switching loss [9]. Fig.8. shows the block diagram for the pulse generation using VFISPWM. Fig.7. and Figs.9. & 10 show the simulated output voltage waveforms and harmonic spectrums of the conventional ISPWM and the proposed MFISPWM for $m_a = 1.00$ and $V_{dc} = 200V$. As it can be seen, the proposed ISPWM technique has always lower THD and the phase voltage waveform shows that the top and bottom levels has less number of switching compared to the conventional ISPWM.
Fig. 7. Simulated Phase Voltage Waveforms for the proposed VFISPWM.

Fig. 8. Block diagram of gating pattern (VFISPWM).

Fig. 9. Output Phase Voltage Spectrum for the Proposed VFISPWM.

Fig. 10. Output Phase Voltage Spectrum for the Conventional ISPWM.

Fig. 11. Variation of THD with modulation index for Fixed frequency (FF) and Variable frequency (VF) ISPWM.

Fig. 12 & 13. shows the simulated closed loop dynamic responses of load voltage and load current of PI controlled multilevel inverter when the load changes from full load (10ohms) to no load (10k) at t = 0.06secs. Fig. 14. shows the dynamic response of load current when the load changes from no load (10k) to full load (10 ohms) suddenly at t = 0.04seconds with P controller[10]. The filter type employed for MLI is resonant arm type filter and the filtered output voltage and current waveform is shown below:
The steady state response of the MLI is shown below:

The performance parameters considered for evaluating the proposed modulation strategy are: spectral quality of the output voltage, THD, WTHD and switching loss [11, 13 -16] which is shown in Table II.

<table>
<thead>
<tr>
<th>S. No</th>
<th>Parameters</th>
<th>Conventional ISPWM</th>
<th>Proposed MFISPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Spectral quality of the output voltage</td>
<td>Lower Order harmonics (3,5,7) are higher</td>
<td>Lower Order harmonics (3,5,7) are reduced.</td>
</tr>
<tr>
<td>2</td>
<td>THD (%)</td>
<td>7.98</td>
<td>5.42</td>
</tr>
<tr>
<td>3</td>
<td>WTHD (%)</td>
<td>0.104</td>
<td>0.076</td>
</tr>
<tr>
<td>4</td>
<td>Switching Loss(mJ/Cycle)</td>
<td>6.38mJ (3950Hz)</td>
<td>2.06mJ (Calculated New Frequencies - 1596Hz, 3443Hz and 3950Hz)</td>
</tr>
<tr>
<td>5</td>
<td>THD(%) (PI CONTROL) Transient state – R = 10KΩ to 10Ω</td>
<td>3.29</td>
<td>1.62</td>
</tr>
<tr>
<td>6</td>
<td>THD(%) (PI CONTROL) Transient state R = 10Ω to 10KΩ</td>
<td>3.69</td>
<td>1.70</td>
</tr>
</tbody>
</table>

It is obvious that VFISPWM technique shows a better performance for the seven-level inverter. The THD of the VFISPWM is shown with PI control which minimizes the amount of harmonics.

V. EXPERIMENTAL RESULTS

A seven-level cascaded inverter has been built using smart power module (SPM - 600V, 23A) IGBTs. One dc source (100V) was used for the single – phase hybrid cascaded MLI and the other source (50V) to generate seven levels. The inverter was first controlled using fixed frequency ISPWM with the following parameters: ma = 1.00 and mf = 79. FPGA SPARTAN processor is used to implement the gating pattern and PI control. The inverters output line- neutral voltage waveforms for all the three phases are shown in Fig.16.
The prototype inverter (refer Fig.1.) was tested using the proposed VFISPWM with different carrier frequencies as discussed in section-IV of this paper. Specifically, the top and bottom bands had a frequency ratio of 36 while the centre and intermediate bands had a frequency index of 79 and 69. Fig.17. and Fig.18. shows the inverter’s output line-neutral and line-line voltage waveforms using the proposed control method. This control method balances the switching actions and gives a lower value of THD compared to the conventional one.

The type of filter employed for the seven–level inverter is the resonant arm filter and the output of the controlled phase voltage of the multilevel inverter is shown below:

VI. CONCLUSION

Asymmetric cascaded multilevel inverter using two unequal dc sources for each phase requires minimum number of switching devices. An inverted sine wave carrier frequency modulation strategy gives maximum fundamental voltage for a given THD. A variable frequency carrier modulation strategy results in reduced switching losses. Advantages of all the above three methods have been exploited in the proposed technique. The PI controller is tested for regulating output voltage and minimizing harmonics of the chosen seven level inverter. The proposed system has lower THD and lower switching loss as compared to that of conventional multilevel inverter.

REFERENCES


**Biography**

**Mrs. R. Seyezhai** obtained her her M.E in Power Electronics & Drives from Shanmugha College of Engineering, Thanjavur in 1998. She has been working in the teaching field for about 12 Years. She has published 50 papers in the area of Power Electronics & Drives.

**Dr. B.L. Mathur** obtained his M.Tech in Power Systems from IIT, Bombay in 1964. He completed his Ph.D. in 1979 from IISc, Bangalore. His Ph.D. thesis was adjudged as the best for application to industries in the year 1979 and won gold medal. He has been working in the teaching field for about 44 Years. He has published 30 papers in National and International journals and 75 in National and International conferences.