

Simulation Analysis of an Effective Gate Drive Scheme for a New Soft-Switched Synchronous Buck Converter

N. Z. Yahaya, K. M. Begam, and M. Awan

Abstract— This paper proposes a new resonant gate driver circuit for a soft switching synchronous buck converter in a fixed load condition. The switching energy can be fully recovered during current commutation phase in the gate driver while the diode conduction losses in the low and high side switches can be substantially reduced by employing additional L and C resonant in the circuit. Using PSpice simulation, the optimization technique has been studied. From the predetermined pulse width of the generated signals, the optimized resonant inductor current is observed to generate less oscillation and hence lower the switching loss. In addition, an optimized dead time interval is inserted between high side and low side of the transistors in the synchronous buck converter to minimize their body diode conduction losses. The detailed operations of both circuits are analyzed.

Index Terms— PSpice Simulation, Resonant Gate Driver, Soft Switching, Synchronous Buck Converter, ZVS

I. INTRODUCTION

There has been an increasing research in pulse-width modulation (PWM) converter's design especially at high switching frequency. At this level of frequency, it gives the pleasure in fast transient response, reduces the size of components and generates superior power density. However, the switching loss and gate loss will increase tremendously [1]. Most importantly, specific PWM designs are only meant for specific applications. In synchronous buck converter (SBC) circuit, for example, the implementation of gate driver using PWM technique is required. Even though the predictive scheme is available in a chip-based module nowadays, the traditional fixed pulse scheme is still preferred due to its simplicity and easy in the design phase. This also includes the additional soft-switching operation in reducing switching losses. Clearly, there are two parts; one is the gate driver design and the other, the soft-switching technique which will be applied to the SBC circuit. This will increase efficiency and overall performance of the converter.

In this work, a high power MOSFET is used in resonant gate drive (RGD) circuit. In operating at high frequency,

RGD presents many limitations, tradeoffs and drawbacks. The duty ratio, D , dead time, T_D and the resonant inductor, L_r are significant in achieving high frequency gate drive operation. The diode-clamped (DC)-RGD circuit is used in the analyses which is shown in Fig. 1, tested in an inductive load system. It has a full capability in recovering energy in the circuit without producing high dissipation at the input.

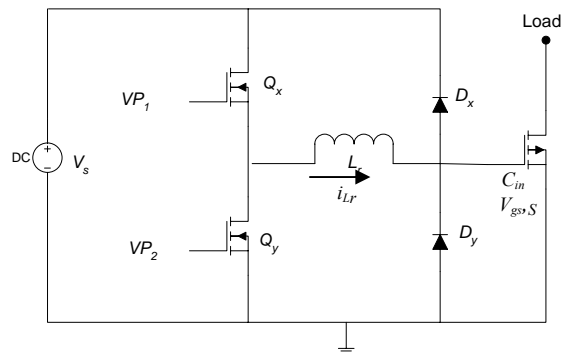


Fig. 1 DC-RGD circuit

In most of RGD circuit designs [2-9], switching losses of the driving switches contribute to the most losses compared to conduction and gate losses. In the circuit, V_{P1} and V_{P2} are the two separate pulse generators which provide complementary square wave signals to either switch Q_x and Q_y . The switching frequency applied is 1 MHz.

In high switching frequency, the switches experience high stress and hence dissipate more heat. Basic work has been reported in [10]. Using proper pulse generation from V_{P1} and V_{P2} respectively, the conduction of Q_x and Q_y will produce the waveforms as shown in Fig. 2. The basic operation of the DC-RGD circuit is as follows. When switch Q_x turns on, the inductor current, i_{Lr} develops. At this time, Q_y is off. Here, i_{Lr} is charged exponentially to maximum value and so is gate voltage of S , $V_{gs,S}$ of which it is clamped to input source, V_s of 12 V.

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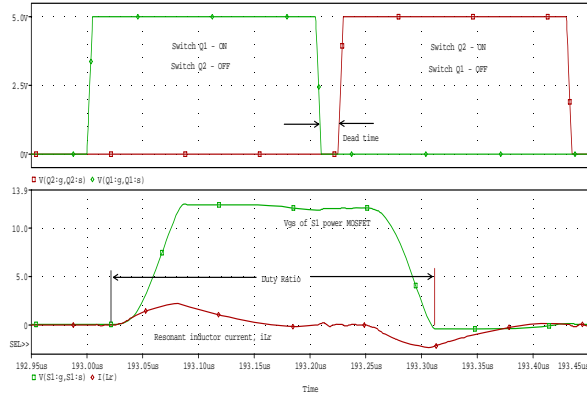


Fig. 2 Operating Waveforms of DC-RGD circuit

The duration of the charging i_{Lr} depends on L_r and the circuit impedance, Z_0 . This is the time constant of the circuit, τ_c (1) where C_{in} is the input capacitance of S . Once $V_{gs,S}$ is fully charged, i_{Lr} starts to discharge to zero through $Q_y, bodydiode-L_r-D_x-V_s$. For a specified time given after Q_x is turned off, Q_y then starts to conduct. This specified time is known as dead time, T_D . The next sequence will show the previously clamped 12-V $V_{gs,S}$ is discharged to zero. This circuit operation repeats for the subsequent cycles.

$$\tau_c = \frac{L_r}{\sqrt{\frac{L_r}{C_{in}}}} \quad (1)$$

A. Limitations & Implications On DC-RGD Circuit

The variation in voltage pulse duration in VP_1 and VP_2 can make difference in operating ratio, D . This determines the length of conduction time of the power MOSFET, S during its turn-on. It is found that D of 20 % (200 ns) being the optimized value for less stress and low dissipation in the circuit [11]. Moreover, each of these pulses must at least have sufficient on-time for i_{Lr} to completely charge and discharge the current.

In other aspect, the higher the inductance value of L_r , the longer current takes to discharge and thus gives rise to ringing in the circuit. The ringing indicates the presence of high harmonic and thus generates higher heat dissipation, leading to possible malfunction in the circuit. The L_r value of 9 nH is determined to be an optimized value to compensate for the trade-offs between speed and switching loss. In addition, by varying T_D , where the time of which both of the switches (Q_x and Q_y) are off, the freewheeling discharged current may increase the switching loss. So, this current has to be minimized and allowed to discharge quickly. Here, an optimized T_D value required to minimize the losses is determined to be 15 ns.

II. PROPOSED RGD CIRCUIT

The proposed RGD circuit will generate two output gate voltages complementarily with a single input voltage source, V_{in} which is suitable for the SBC circuit. The operation of the circuit will utilize the symmetrical behavior of the DC-RGD. As shown in Fig. 3, the left circuit block represents the actual operation of DC-RGD circuit with optimized parameters as discussed previously for Fig. 1. The right circuit block, on the other hand, represents the similar circuit however the T_D between Q_3-Q_4 switches is predetermined differently. The rest of the parameters remain the same.

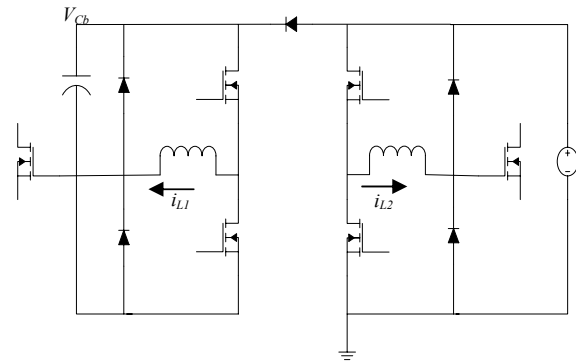


Fig. 3 Proposed RGD Circuit

Also in Fig. 3, there are the additional diode and capacitor, namely, D_b and C_b . They are used for high side drive in SBC being the bootstrap circuit. This circuit has the advantages in circuit simplification, symmetrical behavior and hence minimizes the switching loss. Moreover, it has better immunity in dv/dt turn-on and less impact by parasitic capacitance.

The proposed new RGD circuit consists of four switches Q_1-Q_4 . Both sets of switches Q_1-Q_2 and Q_3-Q_4 behave symmetrically. The inductors, L_1 and L_2 connect the driving switches to the power MOSFETs, S_1 and S_2 which represent the high and low side switch for the SBC circuit respectively. The RGD provides two drive signals with duty cycle D and $1-D$. This is suitable for driving two MOSFETs at a time. The duty cycle for S_1 is D and for S_2 is $1-D$. In both high and low side configuration of the proposed RGD circuit, the independent inductor currents in L_1 and L_2 will flow through the resonant-link train that depend on the conduction of all four switches, Q_1-Q_4 . Since both sets of switches operate symmetrically, the amount of effective resonance effect is approximately equal, and hence the switching loss is controllable. Fig. 4 shows the operating waveforms of the proposed RGD circuit.

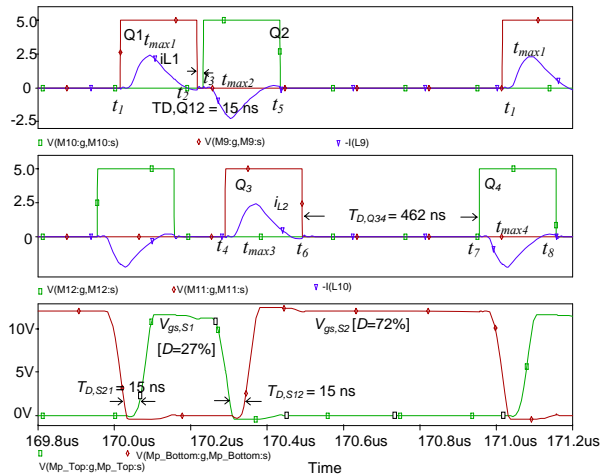


Fig. 4 Operating Waveforms of Proposed RGD Circuit

All of the switches are assumed to be initially off. At t_1 , switch Q_1 starts to conduct. Here, the inductor current of L_1 , i_{L1} charges to maximum at t_{max1} . Then this current will discharge through free-wheeling low impedance path, $Q_2, bodydiode-L_1-D_1-V_{cb}$. The process is the same as described in circuit operation in Fig. 1. This discharged i_{L1} depends on the amount time given by the conduction of Q_1 . In this case,

the duty ratio, D of 20 % is used for the purpose. If the discharging time is insufficient, this gives rise to oscillation of the current at the end of Q_1 turn off at t_2 . This result is not desirable as it leads to higher switching loss.

After a predetermined T_D of 15 ns, the switch Q_2 is then turned on. Q_1 is now turned off. Again, the i_{L1} behaves symmetrically as for the conduction of Q_1 switch. However, at t_3 , i_{L1} again charges to maximum current with negative value at t_{max2} . This value is slightly lower than $i_{L1,max}$ at t_{max1} due to the leakage current during the freewheeling process. Due to the symmetrical behavior of the circuit, at t_4 , Q_3 is turned on. At this time, Q_2 is still conducting while Q_1 is off. With similar fashion, the inductor current, i_{L2} is charged to maximum positive value at t_{max3} . The previous negatively i_{L1} will increase back to zero at t_5 through $D_2-L_1-Q_1, bodydiode-V_{cb}$ as well as i_{L2} decrease to t_6 through $Q_4, bodydiode-L_2-D_3-V_{in}$. During the conduction of Q_1-Q_2 , gate voltage of S_1 , $V_{gs,S1}$ is clamped at V_{in} . For the high side SBC circuit, the duration of the conduction of $V_{gs,S1}$ is from t_1 to t_{max2} which represents D .

The process of resonant inductor current, i_{L2} is identical to i_{L1} . The rest of the operation from t_7-t_8 is the same as for t_3-t_5 . The only difference is that the dead time $T_{D,Q34}$ is set to be 462 ns. This T_D value is optimized for the generation for $V_{gs,S2}$ at $1-D$ from t_4 to t_{max4} and thus, makes it suitable for the low side of SBC circuit.

III. PROPOSED SYNCHRONOUS BUCK CONVERTER (SBC) CIRCUIT

In SBC circuit, S_1 , the high side switch is mainly used for the conversion from high input voltage into a low output voltage at the load [12]. Fig. 5 shows the SBC circuit operating in Zero Voltage Switching (ZVS) condition. The low side switch, S_2 has a longer conduction time compared to S_1 . This is because of the requirement of lowering the conduction loss in S_2 . Since the switches are conducting in complementary manner configured by the RGD circuit, they will not cross-conduct with each other.

During T_D , once S_1 is turned off, the circulating discharged inductor current, i_{L0} at the load will flow into body diode of S_2 while it is yet in off condition. ZVS can be achieved here for this switch. However, S_2 has to be completely turned off before S_1 turns on. When S_2 conducts, it is expected that $S_2, bodydiode$ remains on. In the case of Discontinuous Current Mode (DCM) operation, the negative load inductor current, i_{L0} can be applied where it firstly turn on $S_1, bodydiode$ before the main body of the switch itself. Here, S_1 experiences ZVS condition leading to reduction of switching losses at S_1 [13].

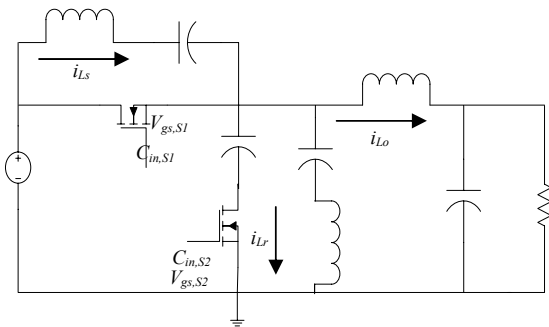


Fig 5 Proposed SBC Circuit with ZVS

Since there is a difficulty in operating SBC circuit within varying load conditions, at all times, S_1 has to turn on with a minimal stress. Here, S_1 must operate at ZVS due to the fact that the i_{L0} variation in either DCM or Continuous Conduction Mode (CCM) operation can alter the state of

switching loss levels. In other words, S_1 is dominant in generating the most loss in the SBC circuit. One way to solve this is by employing additional L_s and C_s components which are connected in parallel to S_1 [14]. The capacitor C_x is used to prevent floating drain voltage of S_1 and the other L_r and C_r are for ZVS operation of S_2 switch. Using this mode, both switches can now be operated in ZVS condition, leading to commutation of discharged i_{L0} through $S_2, bodydiode$ and $S_1, bodydiode$ safely with an effectively lower switching loss. The operating gate and drain voltage as well as drain current waveforms of the proposed SBC circuit are shown in Fig. 6.

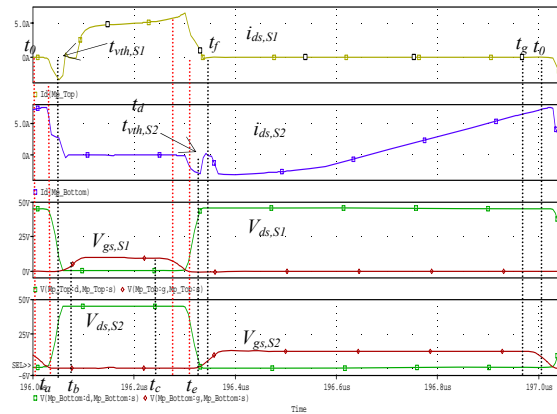


Fig. 6 Operating Waveforms of SBC Circuit

The mode of operation starts at t_a where S_1 is about to turn on (0 V) and S_2 is off. The components used in the simulation are not ideal and they are based on actual specifications provided by the manufacturers. The T_{DS} are set to be 15 ns at (t_a-t_0) and (t_e-t_d) respectively. Since the output inductor current, i_{L0} shown in Fig.7 has negative polarity at the lower peak, it is operating in discontinuous conduction mode (DCM), specifically in light load condition. When S_1 starts to conduct, the negative current of $i_{ds,S2}$ which at peak value will reduce to zero. At this time, S_2 is off. Here i_{L0} increases in a linear fashion. In the complementarily operated mode of SBC circuit, obviously $V_{ds,S2}$ must swing at maximum V_{in} value and $V_{ds,S1}$ at this interval should be zero. This is due to the freewheeling phase of $i_{ds,S1}$ which makes $V_{gs,S1}$ first reaching zero before $V_{ds,S1}$ becomes high.

When $V_{gs,S1}$ reaches its threshold value at $t_{vth,S1}$, $i_{ds,S1}$ starts to develop exponentially until maximum. This current will circulate through L_s and C_s which brings theoretically an additional forward voltage drop of 0.7 V in S_1 leading to $V_{gs,S1}$ of 12.7 V. However, this value is not seen in the simulation. $V_{gs,S1}$ continues to increase to 12 V and remains constant from t_b until t_c .

At t_d , $i_{ds,S1}$ will reach the peak value and this happens when S_1 stops conducting. On the other hand, S_2 is not yet turned on which indicates the interval called “dead time”, T_D . During this time from t_d to t_e , both drain voltage of S_1 and S_2 switches are conducting. Here, $V_{ds,S1}$ increases and $V_{ds,S2}$ decreases. This reflects the decreasing pattern of conducting $i_{ds,S1}$ and $i_{ds,S2}$.

At t_e , $i_{ds,S1}$ is now turned zero. However, due to the decrease of $V_{ds,S2}$ and an increase of $V_{ds,S1}$ at the same time, this makes $i_{ds,S2}$ decrease to maximum negative value. This clearly shows the similar pattern for $i_{ds,S1}$ and $i_{ds,S2}$ for both T_D intervals.

The next sequence shows switch S_2 where it starts to conduct causing $i_{ds,S2}$ back to zero at $t_{th,S2}$. This current will again get back to its previous state before increasing to maximum when S_1 is off, leading to zero $i_{ds,S1}$. $V_{ds,S2}$ is kept constant at V_{in} until t_g where S_2 then starts reducing the value back to zero at t_0 , signaling the decreasing $i_{ds,S2}$ and $V_{ds,S1}$ from the peak and V_{in} , respectively. Then the circuit continues the next switching cycle with the same operating condition.

There shows an identical ZVS operating pattern for S_1 and S_2 with no cross conduction or intersection between both drain and gate voltages. More importantly, the $V_{ds,S1}$ is not floating. Having a nonzero value makes the whole turn-on duration of S_1 experience a higher switching loss as well as to the body diode conduction loss. Using this new SBC circuit, eventually switching loss during S_1 turn on interval can be fully diminished.

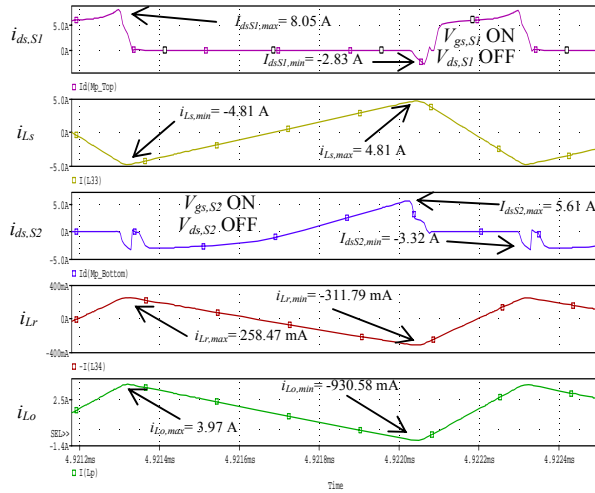


Fig. 7 Inductor Currents of Proposed SBC Circuit

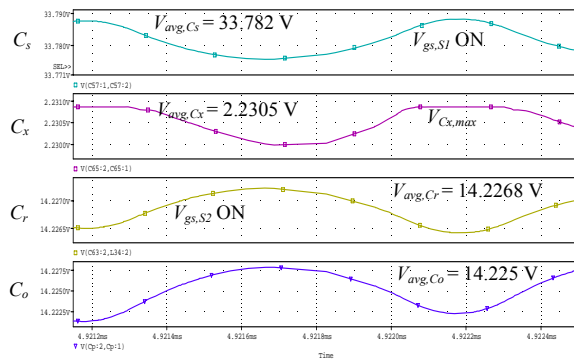


Fig. 8 Capacitor Currents of Proposed SBC Circuit

Fig. 7 and 8 show the inductor currents and capacitor voltages of the proposed SBC circuit. The $L_s C_s$ and $L_r C_r$ pairs are used to commutate i_{Lo} from $S_{2, bodydiode}$ to $S_{1, bodydiode}$ effectively during T_D . Basically the roles of both LC pairs are the same. It can be seen that during T_D , V_{ds} signals for both switches operate in exact complementary fashion. This will minimize the diode conduction losses. Furthermore, L_s and L_r help charged/discharged of $i_{ds,S1}$ and $i_{ds,S2}$ to freewheel completely in each of the switch's conduction cycle, and hence reduce the turn-on switching losses.

The output inductor peak current, $i_{Lo,max}$ is much larger than $i_{Ls,max}$ and $i_{Lr,max}$, indicating the criterion to achieve ZVS condition [15]. The drain voltage floating issue has been resolved by maintaining zero voltage during S_1 turn-on. A capacitor C_x is added in series with S_2 to clamp $V_{ds,S1}$ at zero, with the tradeoff of a lower S_2 voltage pulse applied at the gate of SBC circuit by a $C_{x,max}$ value shown in Fig. 8. This does not affect the operation of SBC circuit much except that the gate charge of S_2 used is reduced for the calculation of low-side RGD losses. The output voltage at the load is not affected due to the fact that there is not much difference seen in C_r and C_o . Interestingly, even though additional components are added, the switching losses, body diode conduction losses are reduced. However, the peak i_{Lo} value is slightly reduced at the output of SBC circuit.

IV. METHODOLOGY

The study is based on simulation using Cadence PSpice simulator. There are two basic blocks in design implementation. First, the RGD block, where the proposed PWM circuit employing diode clamped configuration is implemented as shown in Fig. 3. In this configuration, the generation of D and $I-D$ at both switches, S_1 and S_2 respectively are carefully adjusted. The i_{L1} and i_{L2} are used to charge and discharge the $C_{in,S1}$ and $C_{in,S2}$ where they represent the resonant LC network in the driver. Here, the amount of switching losses are optimized as this configuration is fully controlled for effectiveness in $V_{gs,S1}$ and $V_{gs,S2}$ generation phase. In this PWM RGD circuit, four driving n-channel MOSFETs (Phillips PSMN130), five fast recovery diode (1N6392), a capacitor, two inductors, a DC input voltage of 12 V and four independent pulse generators are used. The pulses provide four different sets of 5-V DC square-wave signals to each of the driving MOSFETs with different delays. The settings of each pulse are shown in Table I. The D and L_1 - L_2 used in this network have been optimized with 20 % (200 ns) and 9 H respectively.

TABLE I.

Parameters	V_1	V_2	V_3	V_4
Delay time	15 ns	232 ns	284 ns	955 ns
Pulse width	200 ns			

Second part is the proposed SBC circuit incorporating ZVS implementation which is shown in Fig. 5. The square-wave pulses provided by S_1 and S_2 from RGD circuit will complementarily turn on the SBC circuit with D and $I-D$ respectively. Having any load conditions, the SBC will be able to deliver higher efficiency with low switching losses especially during T_D . In this work, only a fixed load is studied. Lower diode conduction losses in the body diode of S_1 and S_2 indicate better performance in SBC circuit. Two n-channels MOSFETs (IRFP250), a voltage DC source of 48 V, two capacitors, two inductors and a load resistor are used in the SBC circuit. The details are further analyzed in the results section.

V. SIMULATION RESULTS & ANALYSES

Both proposed RGD and SBC circuits are simulated in this work. A common RGD circuit is used as the test circuit for evaluating the performance of three different SBC circuit topologies with modified parameters. The RGD circuit is only evaluated based on the charge-based calculations and compared with conventional gate driver. The SBC circuit on the other hands will be studied in terms of their switching losses for three different topologies where similar parameters are used in each of them.

A. RGD Circuit

The proposed RGD is evaluated in terms of total switching losses in the circuit including both S_1 and S_2 gate drive losses. Two sets of totem poled drive topologies are used incorporating bootstrap circuitry in the RGD circuit. From Fig. 3, four MOSFETs are applied to generate pulses at high and low side switches of SBC circuit. Since S_2 gate pulse is much lower than S_1 , this makes total gate drive loss slightly lower in S_2 . The total gate drive loss would be the summation of losses in these two switches. However, the output of SBC circuit is not influenced much by this difference.

The total RGD power losses comprise of the following distributions, namely: body diode conduction losses in the driving switches, gate resistance power losses in RGD, gate drive losses of driving switches and losses occurred in inductor, which is considered to be around 20 mW for V_{in} of 12 V. Assuming that Q_1-Q_4 are of the same type and all voltage drops, V_f of the diodes equal to 0.7 V, the distribution of the losses are formulated in equation (2) to (4).

$$P_{bdQ1,4} = 2 \left(\frac{2V_f}{V_{in} + 2V_f} \right) \cdot \frac{Z_0}{R_g + Z_0} Q_{vin} V_{in} f_s \quad (2)$$

$$P_{Rg} = \frac{2R_g}{R_g + Z_0} Q_{vin} V_{in} f_s \quad (3)$$

$$P_{gate} = 4Q_{vin} V_{in} f_s \quad (4)$$

The characteristic impedance of the resonant circuit is

$Z_0 = \frac{L_{1,2}}{C_{inM1,2}}$, Q_{vin} is the gate charge of the driving switches at 12 V and switching frequency, $f_s = 1$ MHz. For $L_{1,2}$ and $C_{inM1,2}$ are determined to be 9 nH and 7 nF respectively, the total gate driver losses are tabulated in Table II.

TABLE II.

Proposed RGD Circuit					
$V_{gs}=12$ V	$P_{bdQ1,4}$	P_{Rg}	P_{gate}	$P_{inductor}$	Ptotal
	5 mW	125 mW	340 mW	20 mW	
Conventional Gate Driver [16]					
$V_{gs}=12$ V	P_{g_chg}	P_{driver}	Ptot_conv		
	1.607 W	0.3 W	1.907 W		

From Table II, it indicates that the proposed RGD circuit can reduce total gate drive losses by 74 % compared with the conventional. The major contributor of losses comes from gate driving switches, P_{gate} . This is different than reported in [16] that gate resistance power losses, P_{Rg} are dominant. As P_{gate} losses are always present in the system and part of the internal structures of devices, the only way to reduce these is by reducing the number of components in the circuit. However, this is not possible. Reducing components will affect the main operation of the circuit. The proposed RGD circuit in this work is found to better leading to an improvement of 3.2 % (506 mW to 490 mW) in total gate drive losses compared to the RGD discussed in [16].

B. SBC Circuit

There are three different SBC circuit configurations used in the simulation. All of them employ the same RGD circuit topology for the purpose of consistency in the analyses. Fig. 9 shows the conventional SBC, the circuit developed by [14] is shown in Fig. 10 and the proposed circuit, Fig. 5. The distribution of parameters for all SBC circuits is shown in Table III.

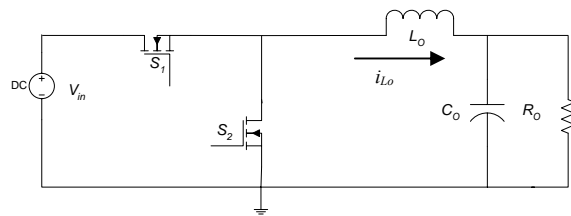


Fig. 9 Conventional SBC Circuit

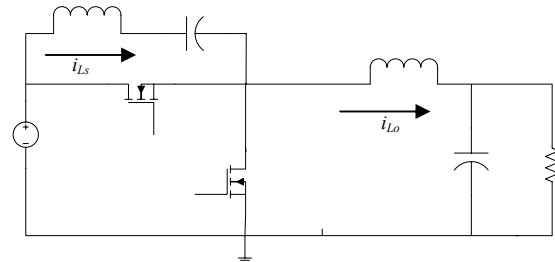


Fig. 10 SBC Circuit Proposed in [14]

TABLE III.

Part Number	Fig. 5	Fig. 10	Fig. 9
V_{in}	48 V		
L_s	0.9 uH		-
C_s	100 uF		-
C_x	1 mF	-	-
C_r	95 uF	-	-
L_r	15 uH	-	-
L_o	1.8 uH		
C_o	100 uF		
R_o	10 Ω		

In Table III, the proposed circuit has more components. This is for the solution to the floating drain voltage of S_1 issue during turn-on which increases switching losses. Fig. 11 shows the portion of turn-off switching losses of all three SBC circuits for S_1 switch. Fig. 13 indicates that by having a floating drain voltage for circuits in Fig. 9 and 10, the turn-on switching losses of S_1 are huge. Conventional gate driver circuit cannot be compared in either during turn-off or on for S_1 and S_2 because of their mismatch in drain voltage switching transitions. So it can be omitted in the analyses. The switching losses during both switching transitions are tabulated in Table IV. The switching power loss is calculated using simple formula: $0.5 * \text{switching time} * \text{peak power} * f_s$.

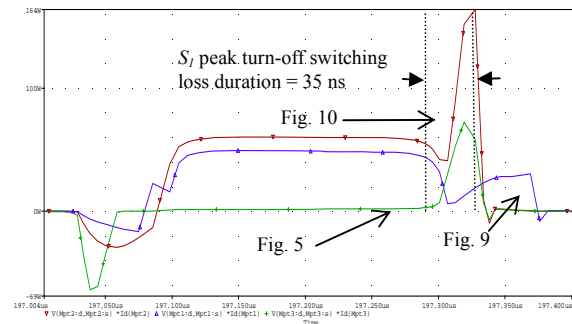


Fig. 11 Turn-Off Switching Loss of S_1

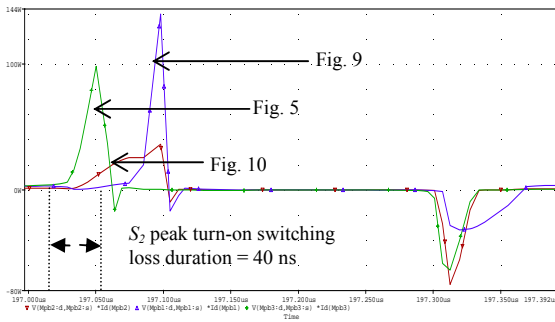


Fig.12 Turn-On Switching Loss of S_2

TABLE IV.

	Fig. 10	Fig. 5	Loss savings
S_1 Turn-off Peak $V_{ds} * I_{ds}$ (Fig. 11)	164 W	65 W	60 %
S_1 Turn-off Switching Losses	2.87 W	1.138 W	60 %
S_2 Turn-on Peak $V_{ds} * I_{ds}$ (Fig. 12)	undefined	95 W	-
S_2 Turn-on Switching Losses	undefined	1.90 W	-

The switching losses presented in [14] differ from the findings in this work due to different parameters settings. Despite of the difference, the analyses are still valid. Comparing the turn-off switching loss of S_1 , the proposed resonant SBC circuit shows a remarkable improvement of 60 % in loss savings with the expected reduction in turn-on switching loss. Turn-on switching losses for Fig. 10 are not able to measure due to the mismatch. In addition, looking from Fig. 12, the entire switching losses of S_1 for Fig. 9 and 10 during turn-on interval are excessively high, which can be clearly seen.

The ZVS behavior during turn-on and off is also important in determining the efficiency and reliability to the SBC circuit. Fig. 13 to 15 show the V_{gs} and V_{ds} waveforms for all three SBC circuits. Based on the parameter settings used in this work, it is determined that the circuit introduced in [14] does not comply entirely with the ZVS condition and in addition, there exists a floating drain voltage of S_1 , leading to high switching losses during its turn-on switching cycle. The rising edge of $V_{ds,S1}$ is also not equal to its falling edge. These losses also occur in the conventional and not in the proposed SBC circuit.

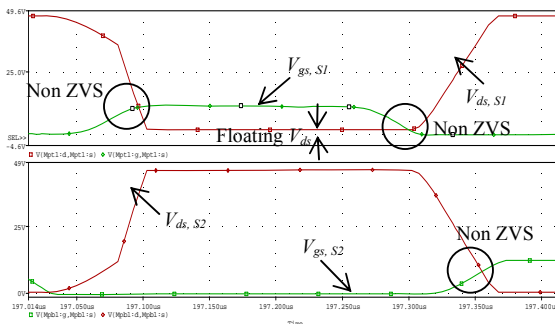


Fig. 13 V_{gs} & V_{ds} of Conventional Gate Driver Circuit

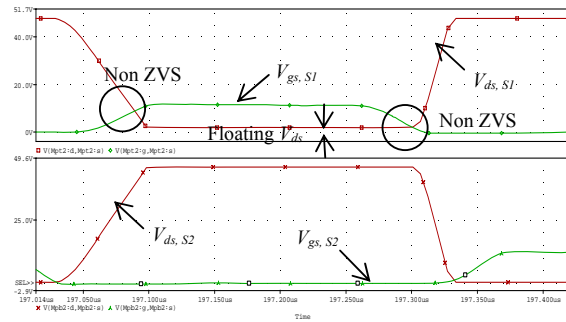


Fig. 14 V_{gs} & V_{ds} of RGD Proposed in [14]

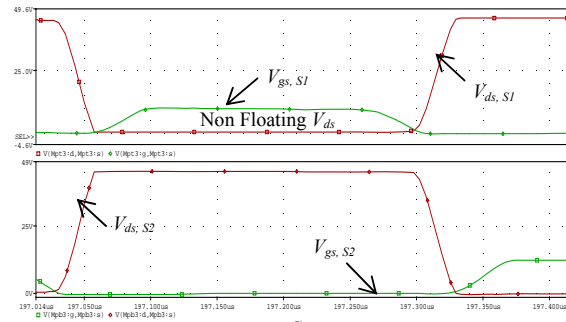


Fig. 15 V_{gs} & V_{ds} of Proposed RGD

The last analysis discusses about the i_{Lo} performance in the SBC circuit. Fig. 16 shows i_{LS} , i_{Ls} , and the three i_{Lo} currents which correspond to V_{gs} of S_1 and S_2 .

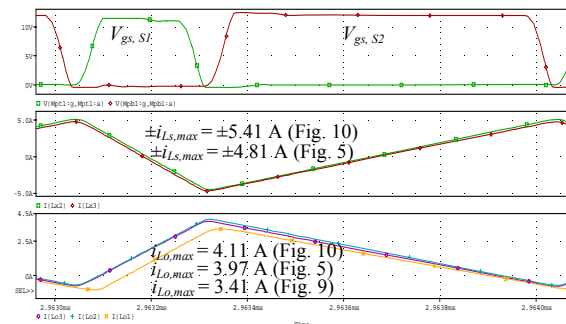


Fig. 16 Comparison of i_{Lo} of Three Gate Driver Circuits

The additional LC configuration which is connected in parallel with S_2 in the proposed RGD circuit slightly influences the i_{Lo} of the SBC. This is true since an additional current is branched out from the source to the node leading to a drop in i_{Lo} at the load. Comparing with Fig. 10, i_{LS} peak in the proposed SBC circuit drops 11 % from 5.41 A to 4.81 A and only 3.4 % in the i_{Lo} . This indicates the drawbacks in the design. However, the circuit has improved the switching losses in S_1 and S_2 despite of the loss in i_{Lo} .

Design compromise has to be made between switching losses and peak i_{Lo} current at the load. With RGD circuit, i_{Lo} is charged and discharged with constant peak value. Therefore, the switching time can be reduced leading to lower switching losses. In addition, more power savings in the body diode conduction losses are achieved in S_1 and S_2 during T_D .

VI. CONCLUSIONS

This paper discusses the importance of switching losses reduction in resonant gate driver (RGD) and synchronous buck converter (SBC) circuits. A RGD circuit is proposed for a new soft switching SBC in a fixed load condition. Using optimized parameter values for the RGD circuit, high (S_1) and low side (S_2) switches of SBC circuit can be generated efficiently. Using PSpice simulation, the gate driver losses improve by 74 % compared to the conventional RGD circuit. On the other hand, the diode conduction and switching losses of S_1 and S_2 are reduced significantly using the proposed SBC circuit. It is found that the proposed SBC circuit increases the loss savings by 60 % compared to the circuit reported in [14]. In fact, the power savings are much higher than the conventional. Due to the additional of LC components used in the proposed SBC circuit, peak output current, i_{Lo} reduces slightly. Despite of this issue, the switching losses of SBC circuit during S_1 turn-on and S_2 turn-off have managed to reduce significantly, leading to less power dissipation. Nevertheless, more work has to be done in getting a higher i_{Lo} for lower switching loss requirements in both RGD and SBC circuits. The experimental verification will be finalized and presented in other publication.

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